Pixel Tracker Status

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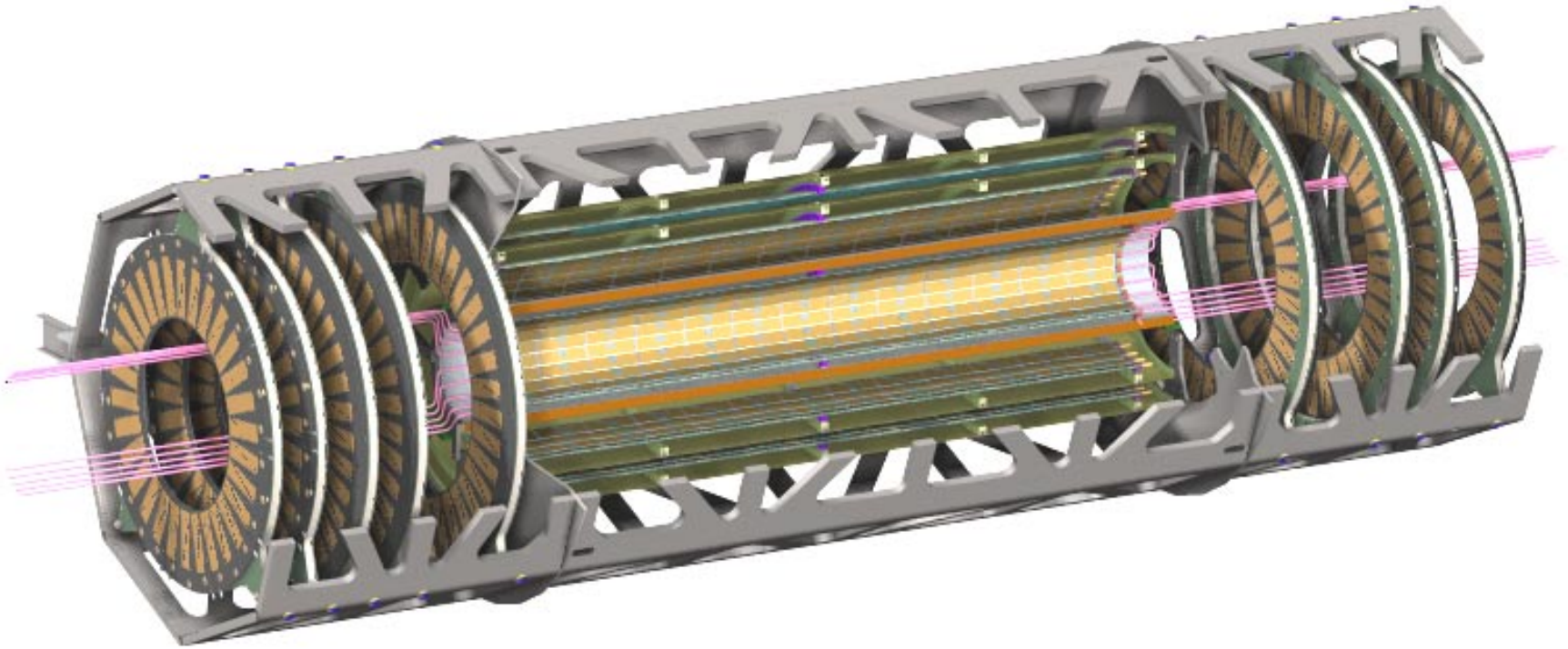
Highlight recent progress and status in all areas:

- **Sensors:** progress towards procurement, new results with oxygenation
- **Electronics:** progress towards rad-hard versions of critical IC's, but TEMIC wafers produced so far do not have acceptable yield.
- **Modules:** progress in module issues related to bumping, thinning, and hybrids.
- **Mechanics, Cooling and Services:** design now mature, prototypes look good, and first system tests of cooling were successful.
- **Layout:** modest updates for new beampipe design.
- **Summary:** preparing for US ATLAS Baseline Review in November

Introduction

Overview of Pixel Tracker:

- System designed to produce three measurement points over full rapidity range $\eta<2.5$ using three barrel layers plus 5 disks located at each end, and all fitting neatly inside the barrel SCT:



- Basic ingredient is pixel module, containing 16FE chips on a common sensor substrate segmented into 46K pixels with a total active area of 10 cm^2.
- Complete detector contains approximately such 2150 modules.

Sensors

Recent developments:

- Sensor design finalized, and “sensor 2” final prototype run fabricated with two vendors. First results on assemblies fabricated with these sensors now exist.
- Progressing towards procurement. Passed FDR (12/99) and PRR (2/00), call for tender initiated 5/00, results expected by the end of this month.
- **Sensor 2 designs:** Emphasis on final wafer layout, significant orders to exercise vendors and allow us to build a large number of modules. Uses latest technology, including moderated p-spray and 50% of wafers oxygenated using ROSE recipe.
- **Oxygenation:** Technique involves diffusion into wafers for 16 hours at 1150 C in O atmosphere. Only useful when irradiation is predominantly charged particles (neutron damage un-affected). Two major effects (other properties unchanged):
- Modification of reverse annealing behavior by “saturating” the total reverse annealing. This gives about half depletion voltage for a fixed large dose. For the B-layer, this roughly doubles lifetime dose (ignoring trapping effects).
- Increase of reverse annealing time constant by about 4. This gives reduced effect of room temperature exposure on irradiated sensors, and considerably relaxes access scenarios. It also allows operation at slightly higher temperature, easing cooling problems. Largely understood in terms of defect phenomenology.

Final Sensor Design (Sensor 2)

- Final design uses small gap n+ in n with p-spray isolation, includes bias grid for testing (hold all pixel implants at ground for I/V tests) and to keep unconnected pixels from floating to large potential in case of bump-bonding defects. It uses "moderated" p-spray to improve pre-rad breakdown voltage (better yield).
- Sensor 2 wafer layout has 3 module tiles ("no dot", "small dot", and "large dot" bias structures) and many test structures in 4" wafer:

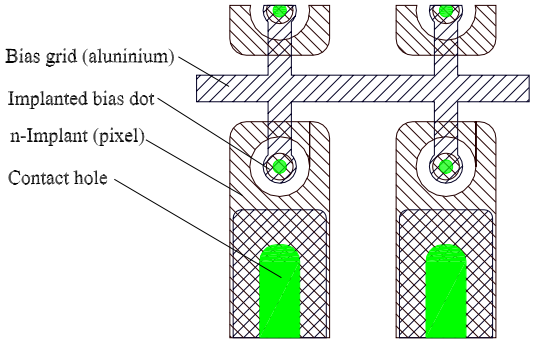
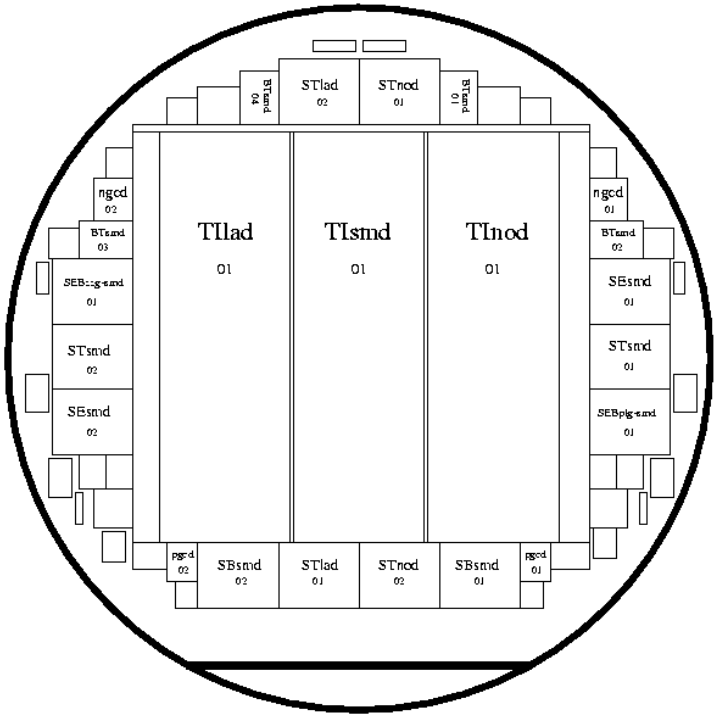
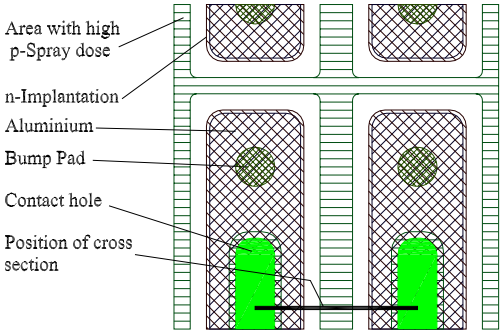
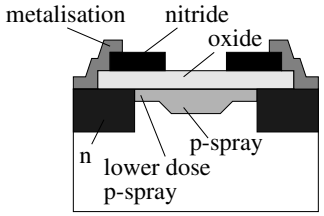


Fig. 10. Design detail of the bias grid in the second sensor prototype.



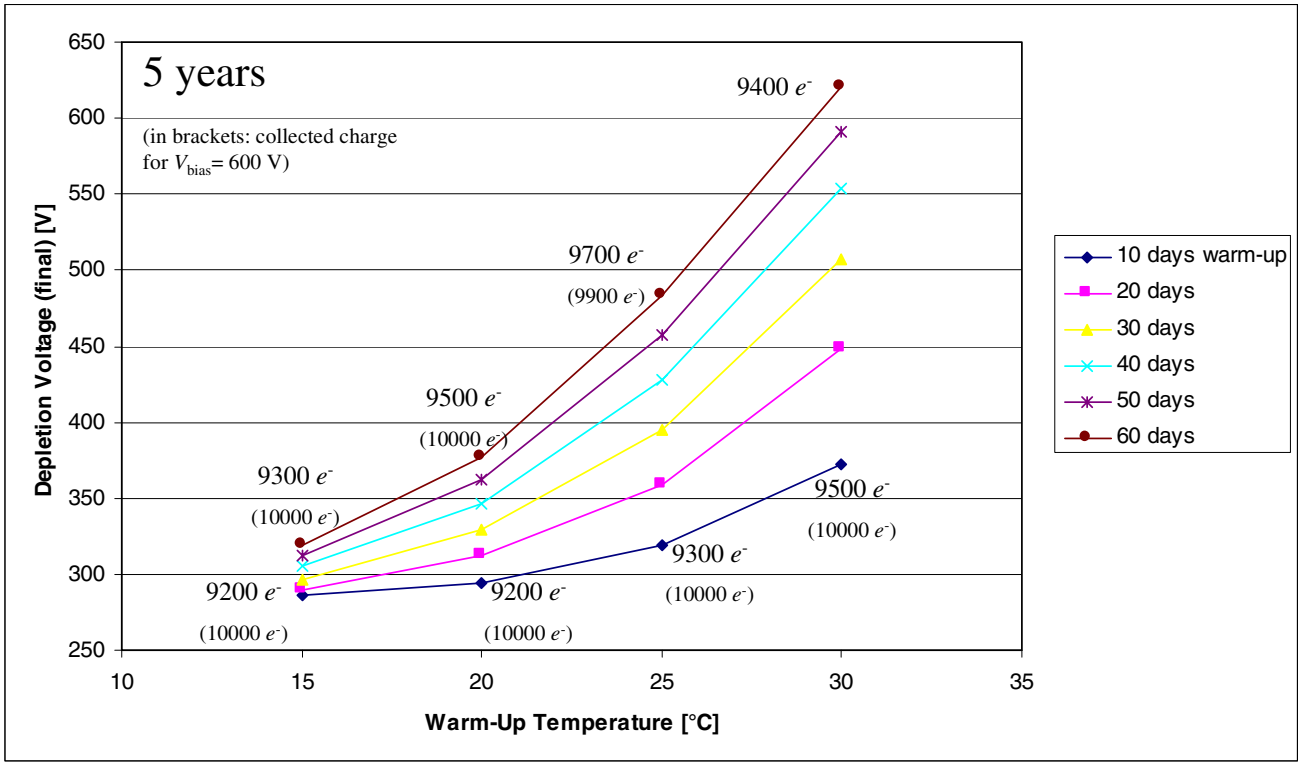




Oxygenated Silicon

Projections for signal for B-layer operation with 5 year dose:

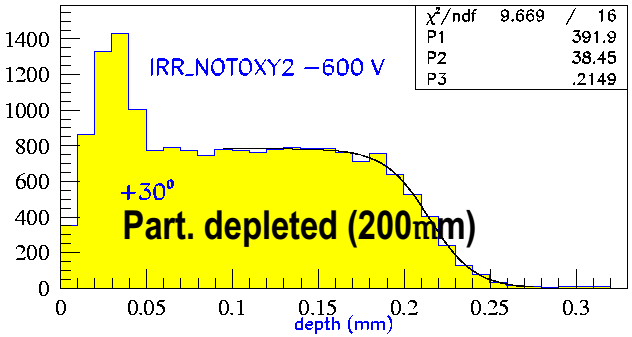
- Radiation level for B-layer: Φ_{eq} (5 years) = 1.2×10^{15} cm^{-2}
- Scenario: 100 days beam at 0°C, *n* days warm-up at *T* per year, rest at -10°C
- Sensor thickness 200µm, oxygenated silicon, $V_{bias}=V_{depl}+50$ V, max. 600 V



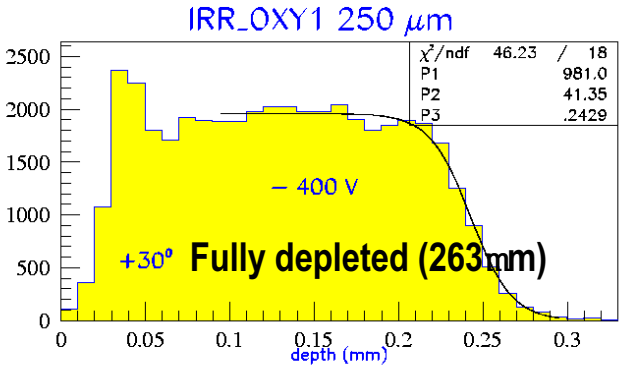
- Stated requirement for electronics is 10Ke signal for full efficiency, so even with operation at 0C and significant warm-up, 5 year operation looks possible.

First Test Beam Results

- First tests with irradiated single chip sensors in H8 in June.
- Additional tests, including single chips with full lifetime dose, just completed last week in H8.



Not-Oxy



Oxy

Comparison of oxygenated and non-oxygenated after 5.6 10^{14} n/equiv.

- Measure depletion depth by using tracks at large incidence angle to extract cluster length.
- Compare two sensor types after irradiation to about 6x10^{14} n-equiv. (lifetime dose for outer layers).
- As expected, get significantly better performance with oxygenated sensors, with full depletion at 400V bias, compared to partial depletion at 600V bias for standard sensor.
- Detailed quantitative studies underway.

Electronics

Electronics components of rad-hard module:

- **Front-end chip:** Sixteen chips per module, each containing 2880 pixels of size 50μ x 400μ, plus control of internal biassing and readout circuitry to produce zero-suppressed event for each L1 trigger.
- **Module Controller chip:** assembles data from 16 FE chips, and provides module level control functions and interface to opto-electronics.
- **Opto-electronics:** Driver for VCSELs used to transmit data stream back to USA15 (VDC) and decoder for clock and command stream from USA15 (DORIC). CMOS designs based on bipolar designs developed at RAL for SCT.

Conversion from rad-soft prototypes to rad-hard designs:

- Agreed to sequentially pursue designs with the two relevant rad-hard vendors (TEMIC DMILL process followed by Honeywell SOI4 process), to reduce risk.
- Began this effort in July 98, preparing FE-D submission. Engineering run submitted in Aug. 99, including complete FE prototype, and opto-electronics prototypes, plus partial MCC prototype.
- Wafers from this run (now called FE-D1) were tested in Oct. 99. Most design goals were achieved, but there appear to be serious technology problems associated with fabricating our FE chip design.

Summary of FE-D1 Results:

Front-end chips:

- Several design errors found, including capacitor short missed by faulty DRC, and several missing or under-sized buffers in control and readout portions of chip.
- Very poor yield observed (no acceptable quality chips on these wafers). This arises mainly from two circuit blocks, and seems to be a technology problem.
- The first circuit is the 2880-bit shift register used to control the configuration of each pixel (calibration and readout masks, plus TDAC values). The yield in the FE-D1 run for this circuit alone was about 25% (circuit is a few percent of die), but improved to 80-90% in backup run (nominally identical processing).
- The second circuit is part of the readout logic inside of each pixel. One observes malfunctioning pixels, which disturb the readout of a column-pair (320 pixels). The behavior is consistent with one NMOS used to reset a dynamic node having a low off-resistance. Subsequent studies confirmed this theory in detail.

Module Controller chips:

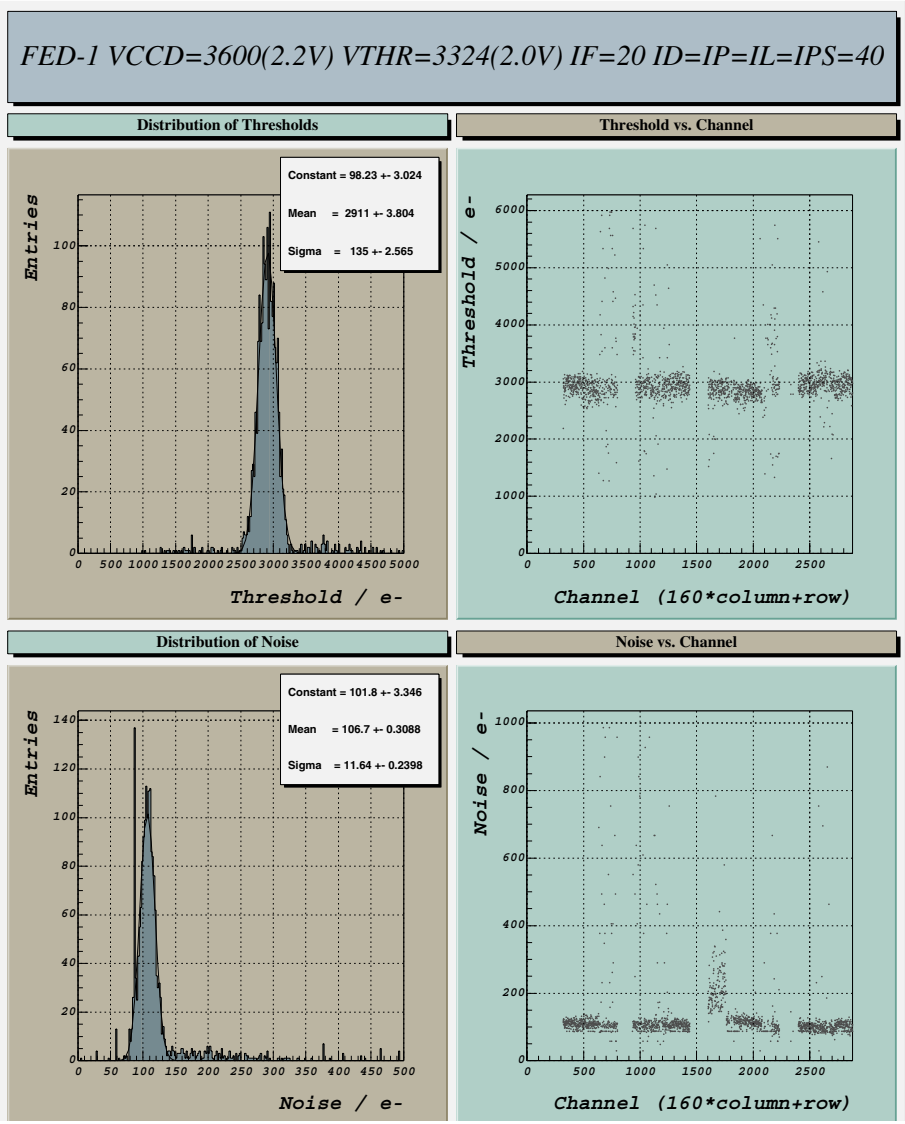
- Performance was as expected, and chips tested successfully to 80-90 MHz. Yield, based on a small number of packaged parts, was about 80%.

Opto-electronics chips:

- VDC worked well. DORIC failed to operate properly at 40 MHz, due to excessive parasitic loading of several critical nodes. Lab behavior reproduced in simulation.

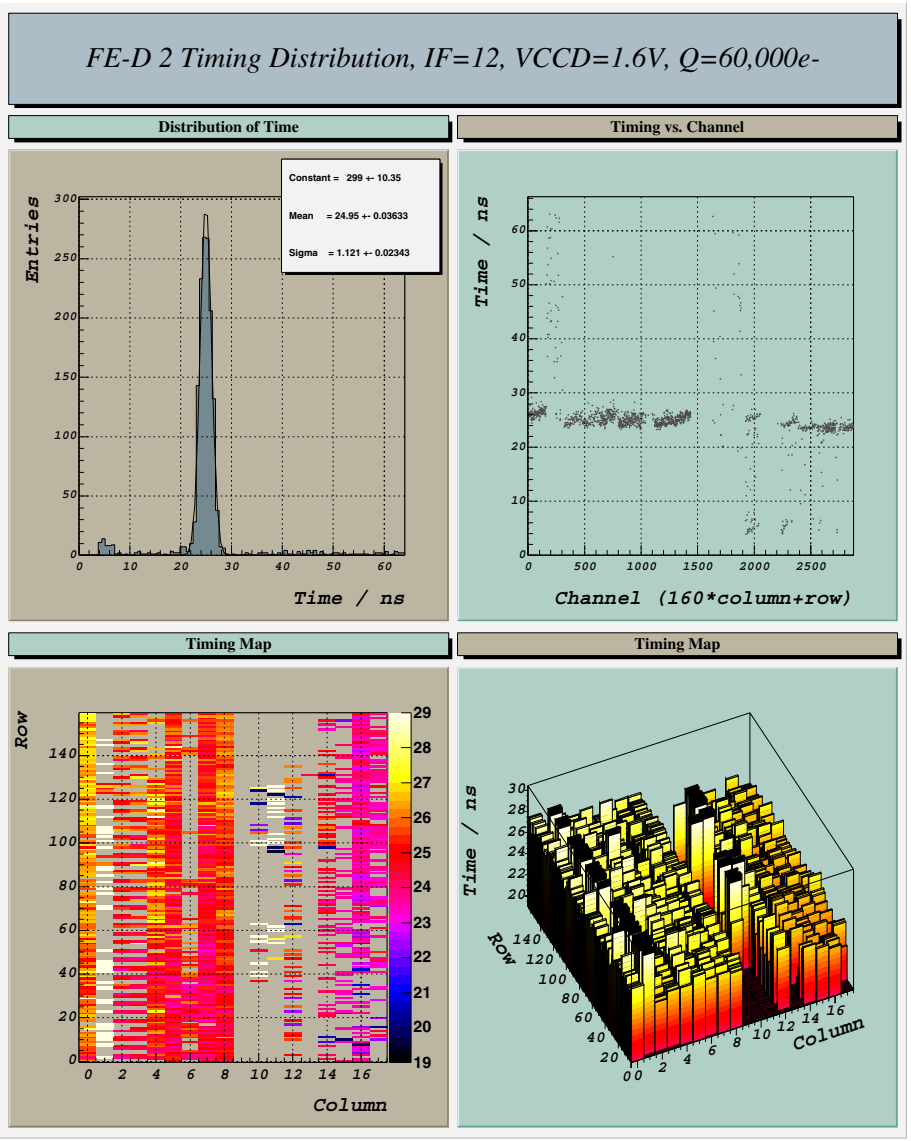
Measurement Highlights:

- Typical threshold scan of good FE-D chip. After tuning, see expected improvement in threshold dispersion (this is a bare chip):



- After tuning, the dispersion is reduced to about 135e.
- The noise is a bit higher than expected, and this is worse still for chips attached to detectors (observe 400-500e noise instead of expected 200e). This is not presently understood.

- Have performed timing studies by injecting a large charge (60Ke) and scanning the delay to find when the hit moves from one crossing to the next:

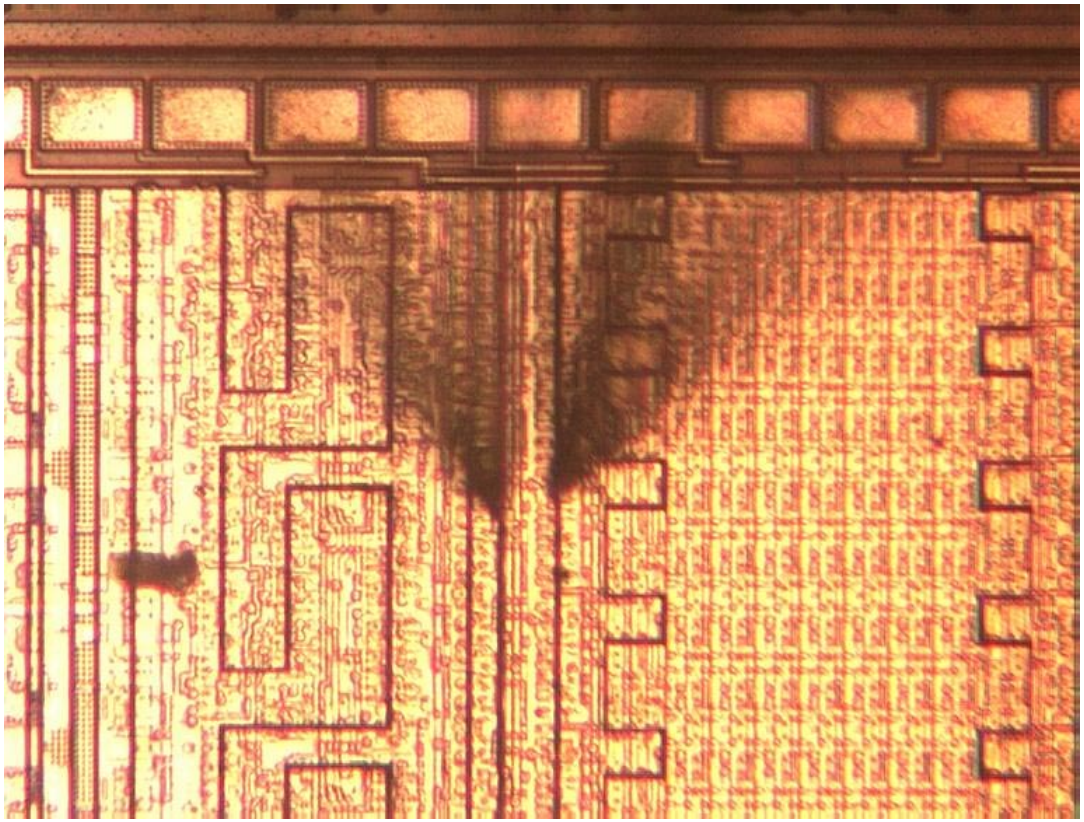


- Some indications of systematic effects, but chip had many bad/ dead channels, so hard to tell.
- Taking an RMS over the channels gives 1.1ns, similar to the results obtained from FE-B in the past.

- Many additional measurements made, including:
- TOT charge measurements with acceptable performance.
- Cross-talk measurements with very good performance (2-3%).
- Timewalk measurements with poorer performance than expected, marginally acceptable.

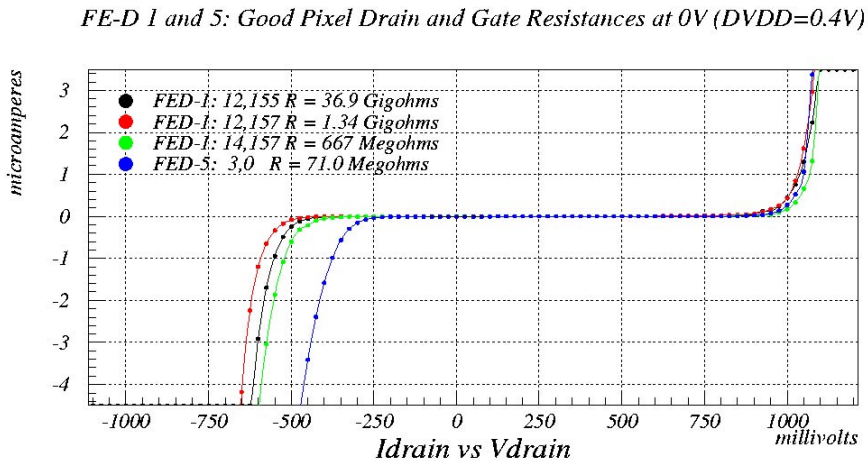
Example of Defect Analysis in Yield Studies

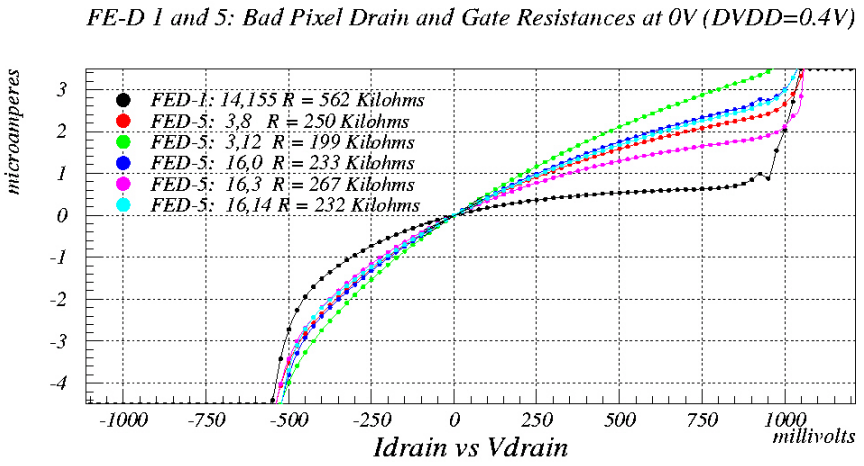
- Two chips which had been characterized in the lab had series of 20 small (8µx8µ) pads deposited by FIB surgery to allow probing of suspect “leaky NMOS”.
- Measurements were made of DC performance of the suspect device (somewhat complex to interpret since they are done in situ), as well as the dynamic performance (using an FET Picoprobe) of waveforms during operation.

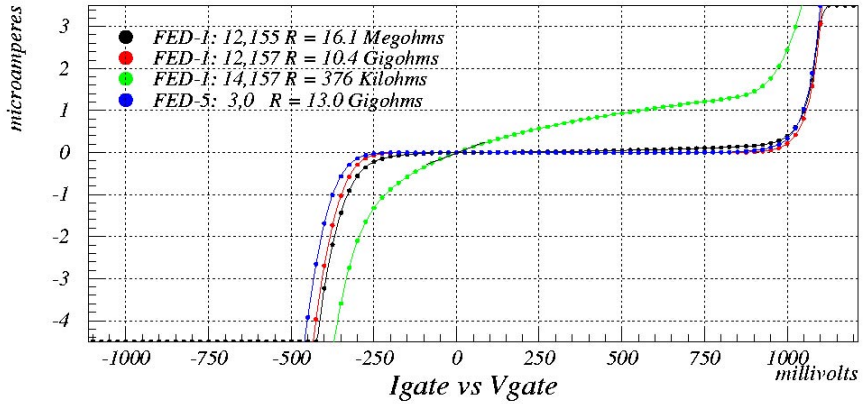


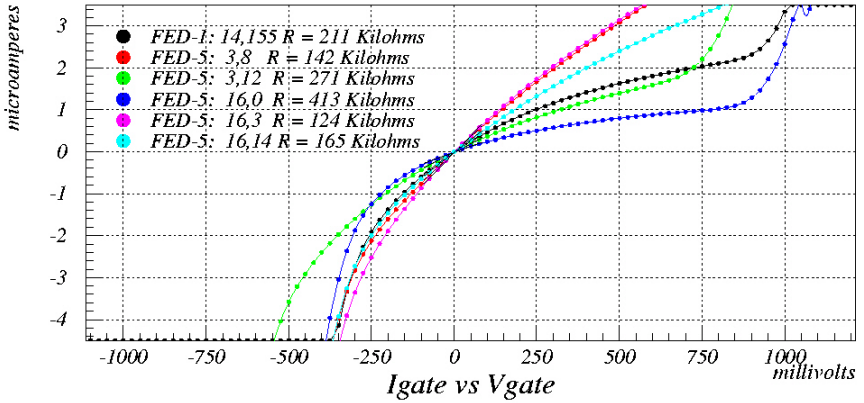
- Two 10µ probe needles place on pads. One pad was on the drain, the second on the gate of the suspect NMOS.

DC curves for pixels previously classified good/bad:



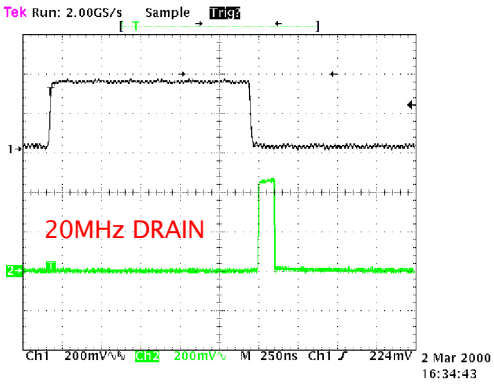


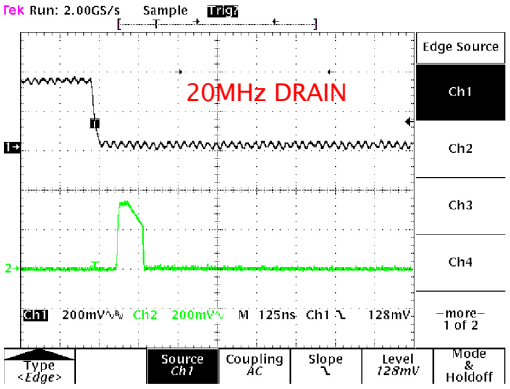


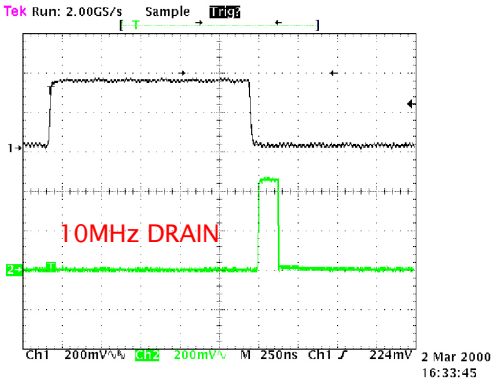


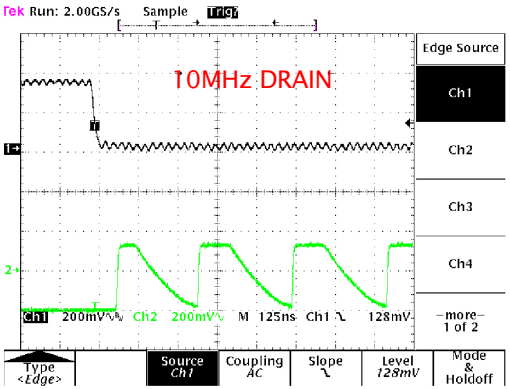
- Bad pixels consistently show apparent drain-source resistance in off state of a few 100's of KOhms. Good pixels show resistance of many orders of magnitude larger, with actual value most likely limited by Tungsten residue after FIB pad deposition.

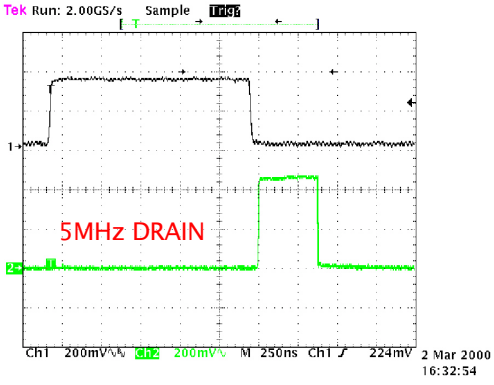
Dynamic measurements of a good and a bad pixel:

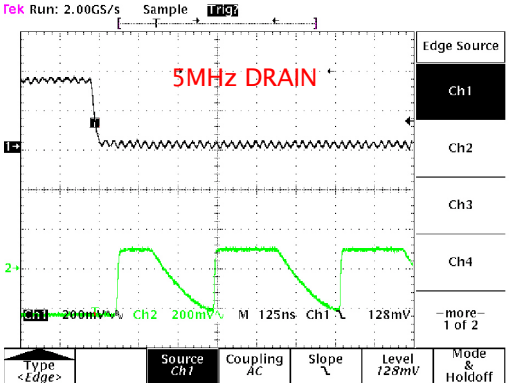












- Measurements of the state of the dynamic node (green trace) were made directly using FET probe (20fF load capacitance).
- Good pixels show stable logic high value over relevant timescale.
- Exponential slope for bad pixel corresponds to dynamic phase when logic value is “leaking” away.
- Depending on clock frequency for column readout, it is possible to produce a “digital oscillation”

Summary of Steps Taken

- Discussion with TEMIC in Jan. 00 meeting in Nantes on how to resolve yield problems. TEMIC performed analysis of defective pixels on two devices, and found no traces of contamination or etch problems that could explain the observed leakage behavior of bad NMOS, also analyzed SIMOX wafers looking for defects.
- TEMIC completed processing on backup wafers from original FE-D1 run, providing us with six additional wafers (FE-D1b). These wafers were processed up to the poly etch at the same time as the original FE-D1 wafers, but processing for many critical steps done later. Compared to FE-D1, they had higher (but still not great) yield on pixel shift register, and similar yield on the readout circuitry.
- Extensive studies of our measurements as well as our layout performed by LETI/CEA (R. Truche, one of process developers), with some resulting suggestions.
- Assistance also from E. Delagne (Saclay, ATLAS LArg). Similar problems were observed in a recent SCA submission. A possible model was proposed, involving problems with poor etching of dense polysilicon traces or contacts located on top of trenches. Recall trenches are a unique feature of DMILL process, and are not completely planar, causing potential problems in processing.
- Such structures are present whenever we have low yield in sub-circuits, and are not present when we have acceptable yield, but detailed predictions did not agree perfectly with measurements.

Second DMILL submission (FE-D2)

Design modifications made:

- Prepare a version of FE-D in which all known design errors are fixed, but the basic design is the same, known as FE-D2D (dynamic).
- Prepare a second version of FE-D in which, in addition, a static version of the pixel register and the readout logic is used. This required additional space, and so the three TDAC bits were dropped from each pixel. This is FE-D2S (static).
- Prepare modified VDC and DORIC chips, in which all known problems uncovered during the testing of the first chips were fixed, and validated in simulation.
- Prepare the full second-generation MCC chip (only completed last week)

TEMIC proposal for FE-D2 run:

- Process a standard 8-wafer engineering run with these designs, but with additional inspection steps for the critical processing of trenches and poly.
- Process an additional full lot (an internal TEMIC run) with significant processing variations in three areas: Leff (critical mask dimension for gate poly patterning), poly etching, and poly contact formation, producing 9 split wafer groups.
- The additional wafers would be made available for us to test to quantify the yield as a function of the process changes. In addition, we have designed special process monitor structures to look for poly processing problems near trenches.

Honeywell HSOI4 submission (FE-H)

- Began work on submission to Honeywell SOI in Fall 99, but most engineering resources were still dedicated to issues related to DMILL.
- This process has significantly higher density than DMILL due to its smaller devices and 3-metal support, allowing us to make a more robust design. Also, the radiation hardness as characterized for single devices appears to be better.
- This design work is now nearing completion, although it is still slowed down by continuing DMILL work (the FE-D2 GDS file was completed only last Friday). We have developed a good technology file and a complete standard cell library.
- We have improved the DMILL design in a number of ways, making it more robust. The critical dynamic elements have all been eliminated, although we continue to believe that they should not have posed any problems in the operation of the design. This means that the design is based on a 50μ x 400μ pixel also.
- We have reformulated the design for the digital logic blocks which do not require full-custom layout, defining them using synthesizable Verilog. This investment improves the rigor of the design, and will ease conversion to a 0.25μ version.
- We hope to submit an engineering run containing two FE chips, the VDC and DORIC, and associated test chips, by early October this year. Unfortunately, the standard Honeywell turnaround time is 5 months, but we are negotiating for some acceleration of this.

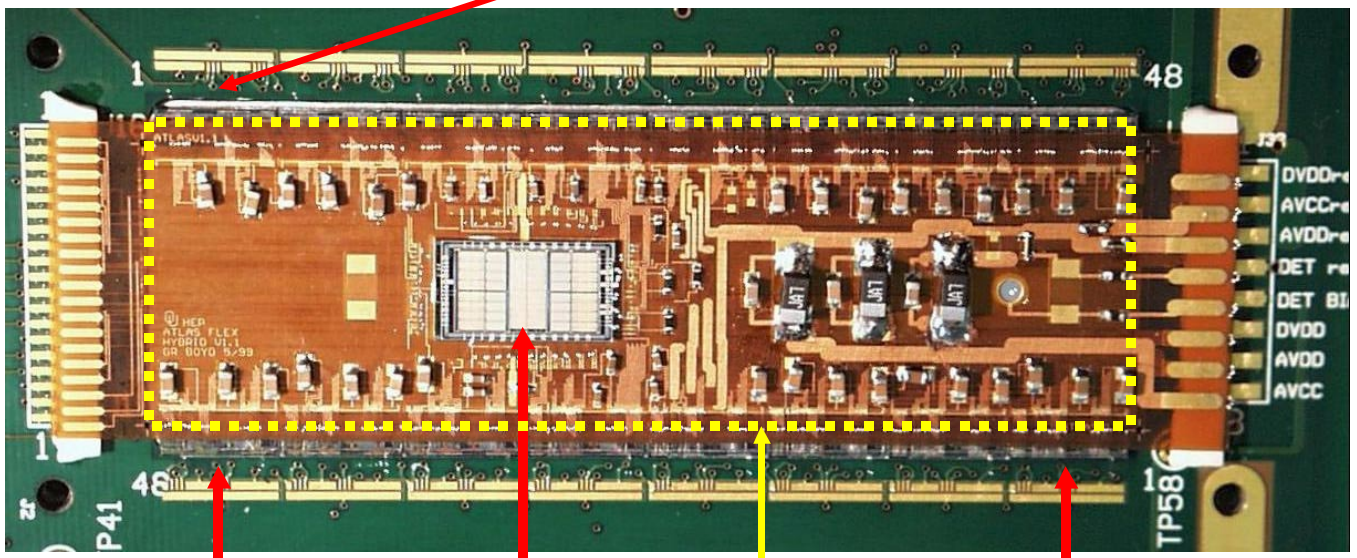
Deep Submicron Plans

- We find ourselves in a situation where our confidence that TEMIC can deliver the approximately 2000 wafers we would need for the present pixel scope is low.
- This requires us to establish a new second vendor to try to contain our risks. In addition, out of our concern about making our design more conservative, we have moved away from the smaller B-layer pixel size which was our original HSOI design goal.
- RD-49 prototyping results with IBM 0.25μ process have been very encouraging, and there are starting to be many significant chips which have been successfully transferred to this process.
- Depending on the outcome of the FE-D2 run, we intend to pursue a conversion to 0.25μ on a rapid timescale, and we have already put into place the necessary NDA, and are studying the design rules and CERN/RAL standard cell library.
- This conversion would initially emphasize the front-end chip, but depending on the results with the opto-link chips from the FE-D2 run (particularly radiation hardness), and the yield and performance of the large MCC-D2 chip on the FE-D2 run, the conversion could be expanded in scope to include the complete set of pixel chips.

Modules

First generation of prototypes built:

- Three bump-bonding vendors IZM (Berlin), AMS (Rome), and Sofradir (Grenoble) used, with significant statistics from first two vendors. Achieve defect rate of 10^{-4}.
- Thinned modules successfully bumped and assembled using FE IC's thinned to 150µ from initial 500µ thickness, and sensors with thickness of 200µ.
- First generation design of Flex Hybrid built by two vendors, and several modules successfully assembled and operated in lab and testbeam.



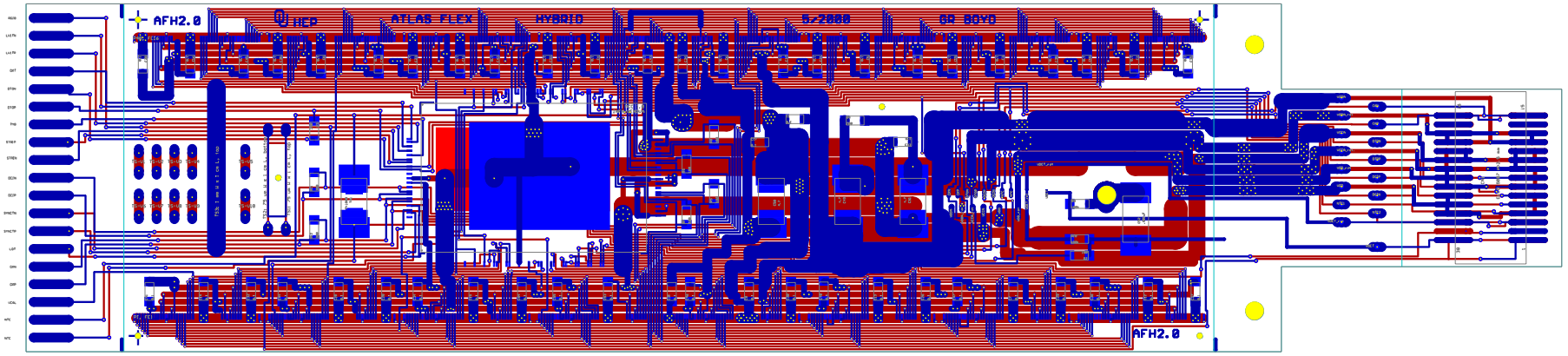
~2 x ~6 cm^2

~0.8 W/cm^2

~1 $kCHF/cm^2$

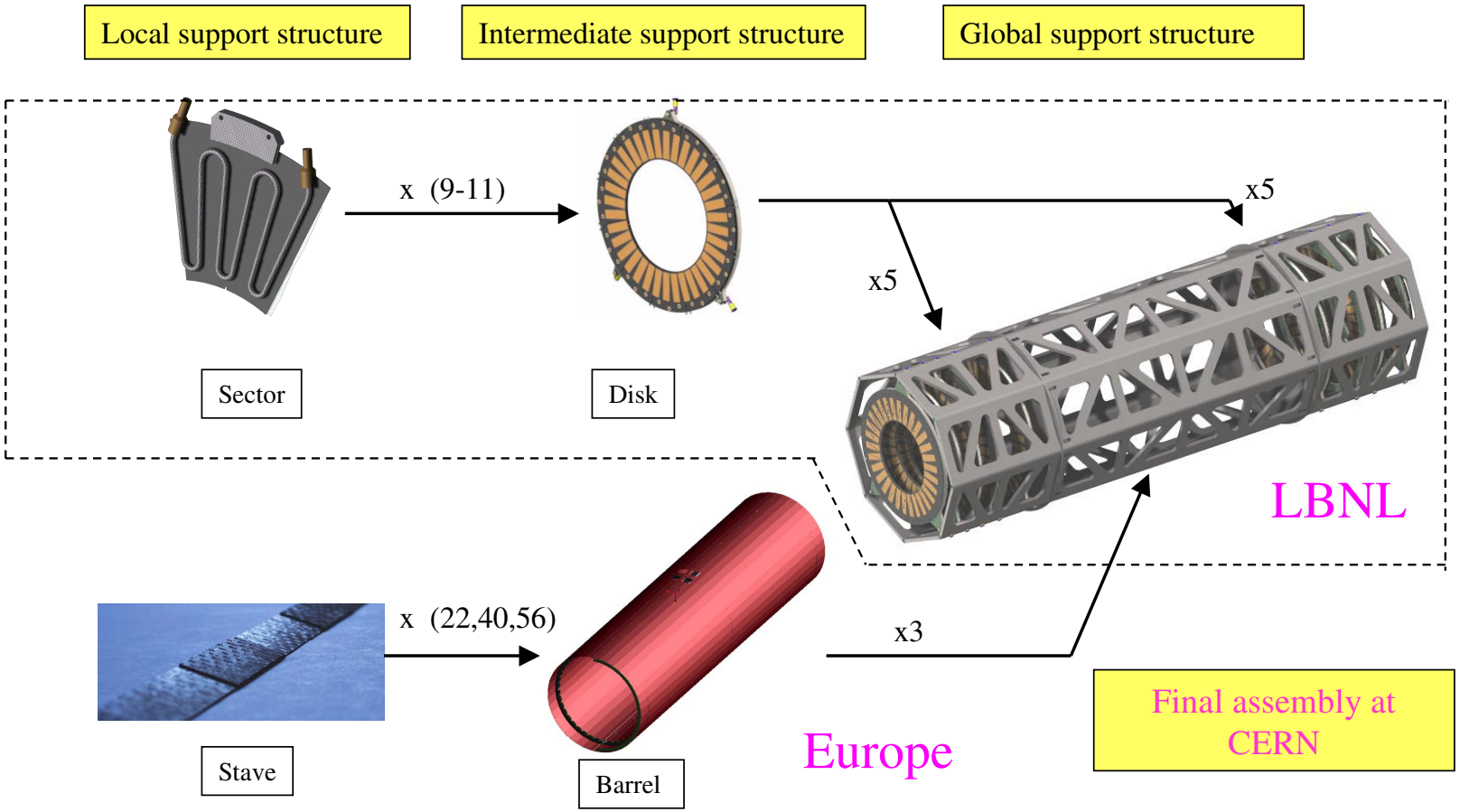
Next generation:

- Prototypes of realistic cable plant, and concepts for patch panel regions exist. Need to exercise modules with proposed 100m cable plant between prototype power supply modules (available in August) and modules to check performance.
- Further prototyping is significantly limited by lack of good quality rad-hard FE chips (we are down to the last wafer of rad-soft chips).
- Second generation Flex Hybrid submitted for fabrication to three vendors (two US, plus CERN). This generation includes conservative components, and prototype pigtail attachments for barrel (side connection) and disk (end connection), plus test connector designed to be cut off when pigtail attached:



- Left end contains “legacy” connections for detailed lab testing. Right end has test connector and pigtail connections. Cut lines shown for barrel and disk versions.

Mechanics status:

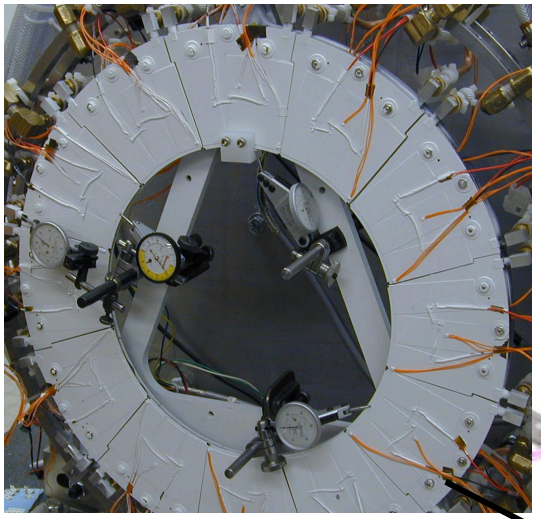


Local supports:

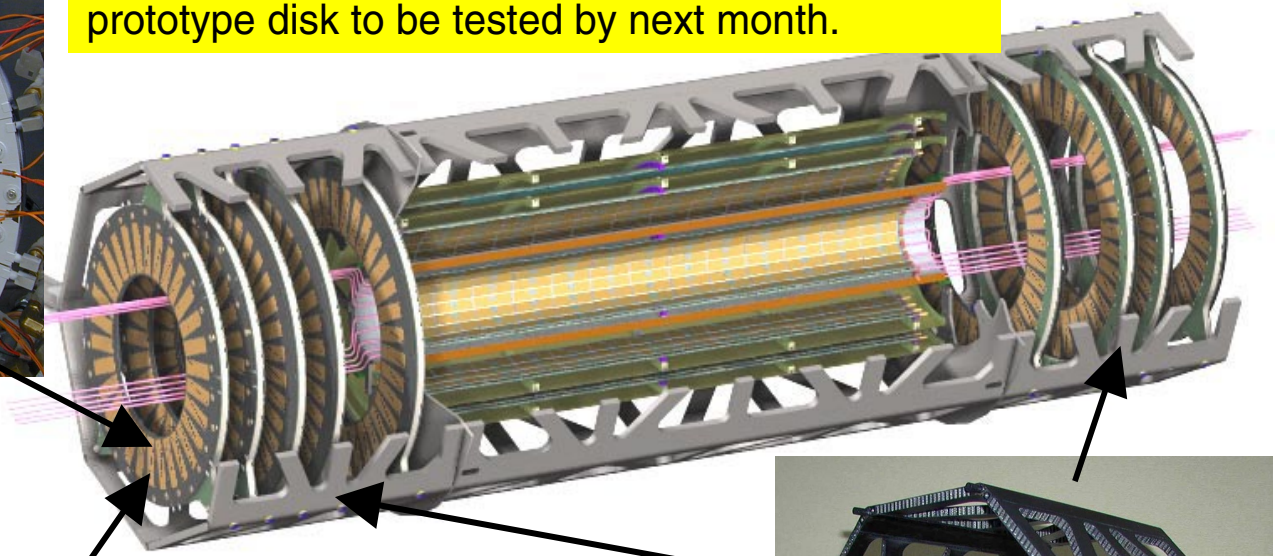
- Many prototypes for sectors and staves built and characterized for mechanical and thermal performance. Designs have recently been upgraded to cope with potential worst-case pressure from C_3F_8 cooling system (8 bar). Local supports passed FDR on June 15 this year.

Global Support:

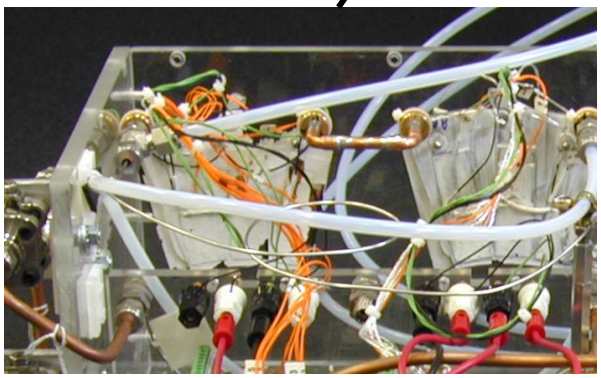
- Prototypes of elements progressing well, including detailed measurements:



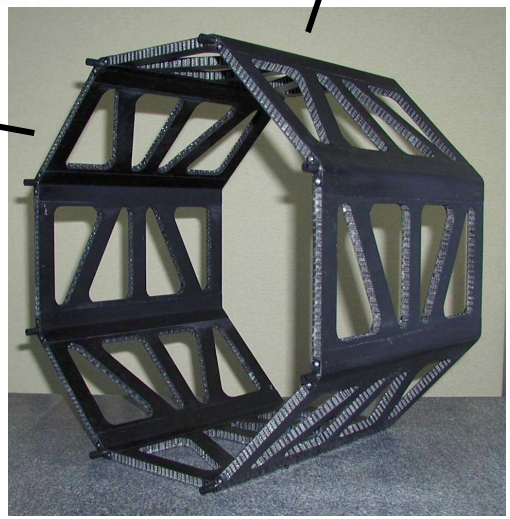
Thermal/mechanical prototype disk fabricated and tested successfully for stability. Second full prototype disk to be tested by next month.



Evaporative cooling tests of disk sectors successfully done.



Prototype end frame section fabricated by December 1999.



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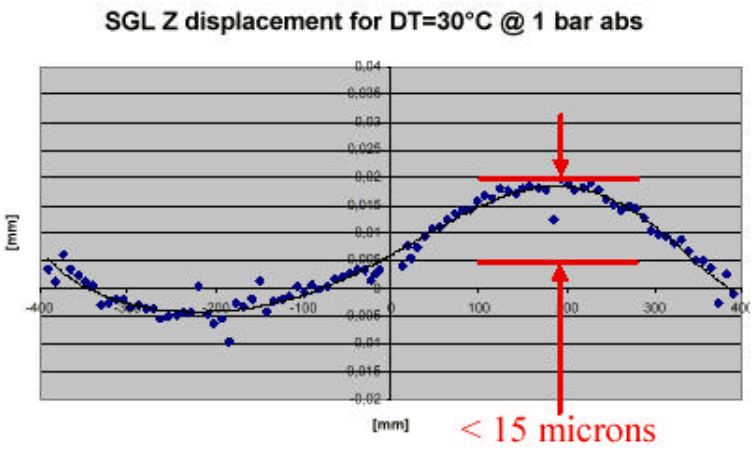
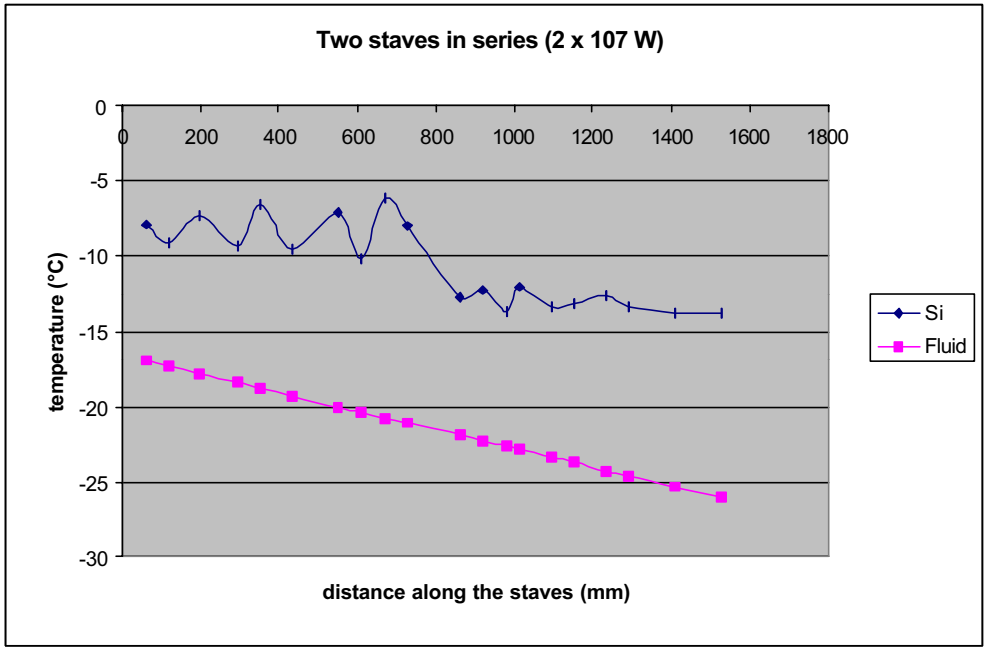
Cooling progress:

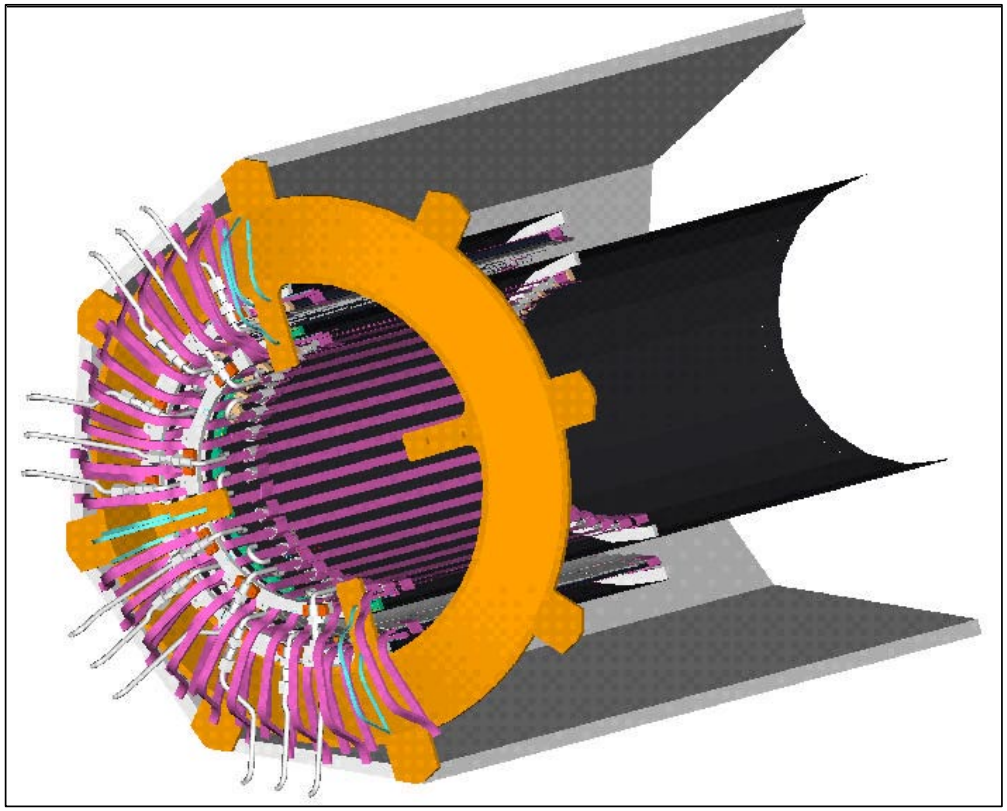
- Review of evaporative cooling design for pixels and SCT on June 15. Outcome was positive. Evaporative system has substantial thermal headroom, but is complex to operate and regulate, so additional operational experience needed.
- Measurements of deflections of stave and sector under thermal cycling from room temperature down to -10C show acceptable behavior.
- Recent system test results performed showing proper cooling operation of two staves in series (baseline modularity) and two disk sectors in series.

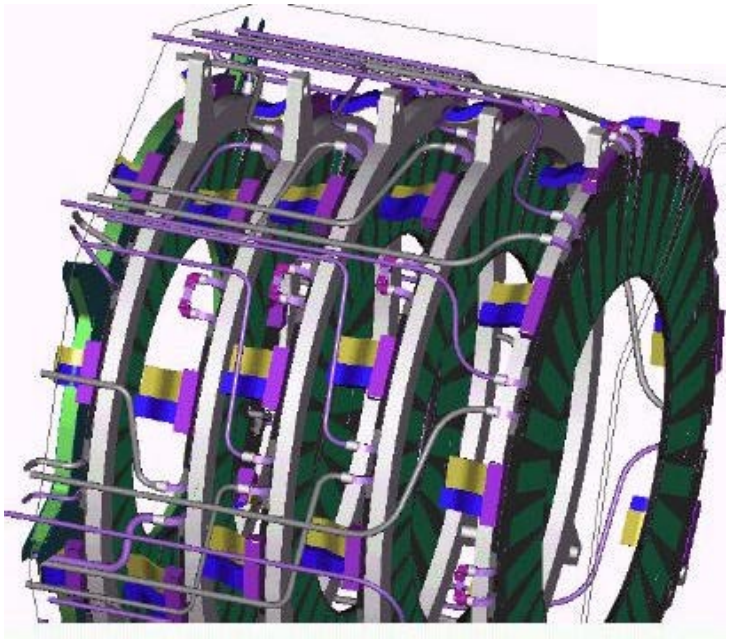




Services status:

- Extensive 3D CAD modeling and design underway. Very complex and over-constrained problem, and real models will also be necessary:





- Critical issues include cooling terminations, and internal “patch panels” to integrate electrical and optical services from half-stave or sector modularity of external harnesses and cables to individual module service connections.

Layout Update

Recent progress in beampipe design and impact on layout

- Beam pipe design now baselined to be double-wall pipe which should allow in-situ bakeout to re-activate distributed getter without requiring removal of B-layer (US proposal). It also should provide a natural mechanism to electrically shield the B-layer.
- This increases the envelope size to a diameter of 72mm, and requires an increase in the B-layer radius.
- The new proposed layout requires 22 staves with a mean radius of 50.5mm and tilt angle of 19 degrees, instead of the previous value of 43mm.
- This is about 17%, and results in a non-negligible degradation of impact parameter resolution (P_T dependent).

First effort to examine fallback options :

- In case there are further delays in electronics schedule, we have formed a working group to study possible responses. In particular, if we have to drop TEMIC as a vendor, there will be a significant delay in our electronics schedule.
- Obvious issues are how to accelerate the construction schedule when electronics becomes available, and exploring how to complete installation of the pixel system into ATLAS at the latest possible date.

Summary

Sensors

- Significant progress towards procurement of production sensors.

Electronics

- Difficulties in making rad-hard conversion are having major impact on schedule. Designs for all required chips are now mature, but vendors are the problem.

Modules

- Progress in bump-bonding, thinning, and Flex hybrid leading towards final module

Mechanics, Cooling and Services

- Excellent progress in finalizing Local Support design and prototyping them.
- Global Support concept prototypes progressing well.
- Evaporative cooling very challenging, but system tests now look functional.

Schedule:

- Electronics delays pose a significant problem for our overall schedule. We have initiated a study group to prepare possible fallback options.
- Baseline review for US ATLAS Pixels is scheduled for Nov 2/3, and we are beginning preparations for this review.